PTO-1449 (Modified)	ATTY. DOCKET NO. RA043D2C6C2	SERIAL NUMBER 09/801,151
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	APPLICANT(S) FARMWALD ET AL.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,330,852	May 18, 1982	Redwine et al.	365	221	
|	4,703,418	Oct. 27, 1987	James	710	32	
|	4,726,021	Feb. 16, 1988	Horiguchi et al.	714	723	
|	4,785,394	Nov. 15, 1988	Fischer	710	44	
TNT	4,870,562	Sept. 26, 1989	Kimoto et al.	711	167	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	S56-82961	July 7, 1981	Japan			YES	
|	S57-14922	Jan. 26, 1982	Japan			YES	
|	Sho 60-80193	May 8, 1983	Japan			YES	
|	Sho 60-55459	Mar. 30, 1985	Japan			YES	
|	S61-72350	April 14, 1986	Japan			YES	
|	S63-142445	June 14, 1988	Japan			YES	
	B63-46864	Sept. 19, 1988	Japan			YES	
TNT	S64-29951	Jan. 31, 1989	Japan			YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
|	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
|	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
|	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
TNT	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER TNT T. NGUYEN	DATE CONSIDERED 11/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,845,670	Jul. 4, 1989	Nishimoto et al.	365	78	
	4,509,142	Apr. 2, 1985	Childers	711	169	
TNT	4,685,088	Aug. 4, 1987	Ianucci	365	189.02	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	0 246 767	April 28, 1987	EPO				
	0 334 552	Mar. 16, 1989	EPO				
TNT	0 276 871	Jan. 29, 1988	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	European Search Report for EPO Patent Application No. 00 101 1832
	European Search Report for EPO Patent Application No. 89 30 2613
	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME" , IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
TNT	JEDEC Standard No. 21C

EXAMINER	TAN T. NGUYEN	DATE CONSIDERED	11/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,649,511	03/10/87	Gdula	711	106	
	4,860,198	08/22/89	Takenaka	710	127	
	3,969,706	07/13/76	Proebsting et al.	365	189.02	
	4,766,536	08/23/88	Wilson, Jr. et al.	710	121	
	4,998,262	03/05/91	Wiggers	375	356	
	4,757,473	07/12/88	Kurihara et al.	365	189.12	
	4,792,926	12/20/88	Roberts	365	189.02	
	4,811,202	03/07/89	Schabowski	710	127	
	5,034,917	07/23/91	Bland et al.	711	167	
	4,845,664	07/04/89	Aichelmann, Jr. et al.	711	405	
	5,140,688	08/18/92	White et al.	710	600	
	4,747,079	05/24/88	Yamaguchi	365	189.08	
	5,301,278	04/05/94	Bowater et al.	711	5	
	5,051,889	09/24/91	Fung et al.	711	157	
TNT	5,153,856	10/06/92	Takahashi	365	233	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	M. Horowitz et. al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987)

EXAMINER	TAN T. NGUYEN	DATE CONSIDERED	11/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,445,204	04/24/84	Nishiguchi	365	194	
|	4,821,226	04/11/89	Christopher et al.	365	230.03	
|	4,882,712	11/21/89	Ohno et. al.	365	206	
|	4,951,251	08/21/90	Yamaguchi et al.	365	189.02	
TNT	5,107,465	04/21/92	Fung et al.	365	230.08	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	T.L. Jeremiah et. al., "SYNCHRONOUS LSSD PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul,. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
|	L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)
|	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
TNT	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)

EXAMINER	TAN T. NGUYEN	DATE CONSIDERED	11/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	5,206,833	04/27/93	Lee	365	233	
	4,953,128	08/28/90	Kawai et al.	365	194	
	4,970,418	11/13/90	Masterson	327	141	
	4,916,670	04/10/90	Suzuki et al.	365	233	
	4,570,220	02/11/86	Tetrick et al.	710	126	
	4,099,231	07/01/78	Kotok et al.	711	168	
	5,301,278	04/05/94	Bowater et al.	711	5	
	5,140,688	08/18/92	White et al.	395	550	
TNT	5,018,111	05/21/91	Madland	365	233	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
TNT	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,734,880	03/29/88	Collins	711	105	
	4,183,095	01/08/80	Ward	365	189.02	
	4,975,872	12/04/90	Zaiki	365	49	
	5,016,226	05/14/91	Hiwada et al.	365	233	
	5,210,715	05/11/93	Houston	365	194	
	4,928,265	05/22/90	Higuchi et al.	365	189.01	
	4,953,130	08/28/90	Houston	365	203	
TNT	5,251,309	10/05/93	Kinoshita et al.	711	167	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
	E. H. Frank, "The SBUS: Sun's High Performance Bus for RISC Workstations", Sun Microsystems Inc. 1990
	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1118-1128 (Oct 1990)
TNT	J. Chun et al. "A pipelined 650MHz GaAs 8K ROM with Translation Logic" GaAs IC Symposium 1990

EXAMINER	TAN T. NGUYEN	DATE CONSIDERED	11/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
INT	4,630,193	Dec. 16, 1986	Kris	713	502	
	4,710,904	Dec. 1, 1987	Suzuki	365	226	
	4,739,502	Apr. 19, 1988	Nozaki	365	233	
	4,205,373	May 27, 1980	Shah et al.	710	128	
INT	4,905,201	Feb. 27, 1990	Ohira et al.	365	230.03	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

INT	European Search Report for EPO Patent Application No. 00 10 0018
INT	European Search Report for EPO Patent Application No. 00 10 822

EXAMINER	DATE CONSIDERED
TAN T. NGUYEN	7/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	3,691,534	09/12/72	Veradi, et. al	365	78	
	3,771,145	11/06/73	Wiener	365	240	
	4,536,795	08/20/85	Hirota, et. al	348	214	
	4,629,909	12/16/86	Cameron	327	211	
	4,631,659	12/23/86	Hayne, et. al	711	167	
	4,858,113	08/15/89	Saccardi	710	132	
	4,499,536	02/12/85	Gemma et al.	711	167	
TNT	4,648,102	03/03/87	Riso, et. al	375	356	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	EP 0424774	05/02/91	EPO				
TNT	EP 0449052	03/29/90	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Takasugi, A. et al., "**A Data-Transfer Architecture for Fast Multi-Bit Serial Acess Mode DRAM**," 11th European Solid State Circuits Conference, Toulouse, France pp.161-165 (Sep. 1985)
	Amitai, Z., "**Burst Mode Memories Improve Cache Design**," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
	Fagan, J.L., "**A 16-kbit Nonvolatile Charge Addressed Memory**," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5, pp. 631-636 (Oct. 1976)
	Ikeda, Hiroaki et al., "**100 MHz Serial Acess Architecture for 4Md Field Memory**," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
TNT	Schmitt-Landsiedel, Doris, "**Pipeline Architecture for Fast CMOS Buffer RAMs**," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 11/02/07

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,663,735	05/05/87	Novak, et. al	345	533	
|	4,825,287	04/25/89	Baji, et. al	348	720	
|	4,845,677	07/04/89	Chappell, et. al	365	189.02	
|	4,873,671	10/10/89	Kowshik, et. al	365	189.12	
|	4,876,670	10/24/89	Nakabayashi, et. al	365	194	
TNT	4,901,036	02/13/90	Herold, et. al	331	25	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	EP 0218523	05/30/89	EPO				
|	JP-A-1-236494	09/21/89	JP			YES	
|	Sho 62-71428	03/27/87	JP			YES	
TNT	EP 0282735	09/21/88	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Horowitz et al., "**MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache**", IEEE J. Solid State Circuits, vol. SC-22, No. 5, pp. 790-798 (Oct. 1987)
|	Robert J. Lodi et al., "**Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit**," 1976 IEEE International Solid-State Circuits Conference (Feb. 18, 1976)
|	1989 GaAs IC Data Book & Designers Guide, Gigabit Logic Inc. (Aug 1989)
TNT	"IC's for Entertainment Electronics, Picture in Picture System Edition 8.89", Siemens AG, 2/89

EXAMINER Tan T. Nguyen	DATE CONSIDERED 6/02/01

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U.S. PATENT DOCUMENTS

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TNT	4,979,145	12/18/90	Remington, et. al	711	106	
	5,099,481	04/24/92	Miller	371	22.1	
	5,016,226	05/14/91	Hiwada, et. al	365	233	
	5,023,835	06/11/91	Akimoto, et. al	365	155	
	5,036,495	07/30/91	Busch, et. al	365	233	
	5,111,486	05/05/92	Oliboni, et. al	375	376	
	5,123,100	06/16/92	Hisada, et. al	713	401	
TNT	5,276,846	01/04/94	Aichelmann Jr., et. al	711	165	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Svensson, Christer, "**High Speed CMOS Chip to Chip Communications Circuit**," IEEE International Symposium on Circuits and Systems, pp. 2228-2231 (Jun. 1991)
	Wakayama, Myles, "**A 30-MHz Low-Jitter High-Linearity CMOS Voltage-Controlled Oscillator**," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 6, pp. 1074-1081 (Dec. 1987)
	Whiteside, Frank, "**A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output**," IEEE International Solid-State Circuits Conference Digest (Feb. 1986)
	Wu, Jich-Tsorng, "**A 100-MHz Pipelined CMOS Comparator**," IEEE Journal of Solid-State Circuits, Vol. 23, No. 6, pp. 1379-1385 (Dec. 1988)
TNT	Lineback, J. Robert, "**System Snags Shouldn't Slow the Boom in Fast Static RAMs**," Electronics, pp. 60-62 (July 23, 1997)

EXAMINER	Tan T. Nguyen	DATE CONSIDERED	11/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	5,361,277	11/01/94	Grover	375	356	
TNT	5,684,753	11/04/97	Hashimoto, et al	365	219	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	WO 89/12936	12/28/89	PCT				
TNT	JP 62-51509	03/06/87	Japan			YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Graham, Andy and Stewart Sando, "**Pipelined Static RAM Endows Cache Memories with 1-ns Speed**," Electronic Design, pp. 157-170 (Dec. 1984)
	Pinkham, Raymond, "**A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications**," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
	Ishimoto, S. et al., "**A 256K Dual Port Memory**," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)
	Iqbal, Mohammad Shakaib, "**Internally Timed RAMs Build Fast Writable Control Stores**," Electronic Design, pp. 93-96 (August 25, 1988)
	Schnaitter, William M. et al., "**A 0.5-GHz CMOS Digital RF Memory Chip**," IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986)
	Bursky, Dave, "**Advanced Self-Timed SRAM Pares Access Time to 5 ns**," Electronic Design, pp. 145-147 (Feb. 22, 1990)
TNT	Tomoji Takada et al., "**A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories**," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 11/02/01

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
INT	4,763,249	08/09/88	Bomba et al.	713	600	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

INT	Robert J. Lodi et al., "**MNOS-BORAM Memory Characteristics**," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
	Gregory Uvieghara et al., "**An On-Chip Smart Memory for a Data-Flow CPU**," IEEE Journal of Solid-State Circuits, vol. 25, No. 1, pp. 84-89 (Feb. 1990)
	Ray Pinkham et al., "**A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature**," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
	Graham, Andy and Stewart Sando, "**Pipelined Static RAM Endows Cache Memories with 1-ns Speed**," Electronic Design pp. 157-170
	Hans-Jurgen Mattausch et al., "**A Memory-Based High-Speed Digital Delay Line with a Large Adjustable Length**," IEEE Journal of Solid-State Circuits, vol. 23, no. 1, pp. 105-110 (Feb. 1988)
INT	Kanopoulos, Nick and Jill H. Hallenbeck, "**A First-In, First-Out Memory for Signal Processing Applications**," IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)

EXAMINER	DATE CONSIDERED
TAN T. NGUYEN	11/02/01

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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2C6C2	SERIAL NUMBER 09/801,151
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	FILING DATE March 7, 2001	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	SHO 58-192154	Nov. 9, 1983	Japan			NO	
	SHO 63-34795	Feb. 15, 1988	Japan			NO	
	SHO 61-107453	May 26, 1986	Japan			NO	
	SHO 63-91766	April 22, 1988	Japan			YES	
	SHO 62-16289	Jan. 24, 1987	Japan			NO	
TNT	SHO 61-160556	Oct. 4, 1986	Japan			NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	5,179,667	01/12/1993	Iyer	711	167	
	5,029,124	07/02/1991	Leahy et al.	710	105	
	4,878,166	10/31/1989	Johnson et al.	710	127	
	4,851,990	07/25/1989	Johnson et al.	710	100	
	4,839,801	06/13/1989	Nicely et al.	710	35	
TNT	3,950,735	04/13/1976	Patel	710	60	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Motorola MC88200 Cache/Memory Management Unit User's Manual, Motorola Inc. 1989
TNT	B. Ramakrishna et al., "The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Trade-offs" Computer IEEE, Jan 1989 pp. 12-35

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE March 7, 2001	GROUP ART UNIT 2818

DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	"MIPS Chip Set Implements Full ECL CPU" Microprocessor Report, MicroDesign Resources Inc., Vol. 3: No. 12; Dec. 1989
	"R6000 System Bus & R6020 SBC Specification" MIPS Computer Systems Inc., Sunnyvale, CA, Aug 22, 1989
	R.A. Volz et al., "POSITION PAPER ON GLOBAL CLOCK FOR THE FUTUREBUS +", SCL – 1989 – doc-59, pp. 1-9
TNT	"ECL bus controller hits 266 Mbytes/s" Microprocessor Report, MicroDesign Resources Inc., Vol. 4: No. 1; Pg. 12, Jan. 24, 1990

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